This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Add claims 12-17.

Amend claims 1, 9 and 11.

1. (Currently Amended) A digital processor responsive to a microinstruction to perform an operation, the digital processor comprising,

a memory for storing data associated with the operation to be performed;

a finite state machine (FSM) for performing a function in association with the operation; and

control circuitry for providing data to the register and for enabling ~~starting~~ execution of the FSM in response to detecting a predefined value in a field in the microinstruction and for preventing execution of the FSM when the predefined value is not detected.

2. (Original) The digital processor of claim 1, further comprising

loop control circuitry for repetitively accessing the data stored in the memory.

3. (Original) The digital processor of claim 1, wherein the control circuitry includes

ID detection circuitry for determining that at least a portion of a microinstruction is to be implemented by the FSM.

4. (Original) The digital processor of claim 1, further comprising

a plurality of FSMs;

wherein the control circuitry includes

FSM execution circuitry to selectively invoke operation of one or more of the plurality of FSMs.

5. (Original) The digital processor of claim 1, further comprising

a configurable FSM;

wherein the control circuitry includes

configuration circuitry to direct the configurable FSM to be configured for a predetermined function associated with the microinstruction.

6. (Original) The digital processor of claim 1, wherein the memory includes a register.

7. (Original) The digital processor of claim 1, wherein the memory includes a microstore.

8. (Original) The digital processor of claim 1, wherein the memory includes a cache.

9. (Currently Amended) A computer processor for executing a microinstruction, the computer processor comprising

a finite state machine (FSM);

an iterative register; and

control circuitry for controlling the FSM and the iterative register to implement at least a portion of the microinstruction when a predefined value in a field in the microinstruction is detected and for preventing execution of the FSM when the predefined value is not detected.

10. (Original) The computer processor of claim 9, wherein the FSM and iterative register are operated concurrently.

11. (Currently Amended) A method for executing a microinstruction, the method comprising

using both a finite state machine and an iterative register to implement at least a portion of a function indicated by the microinstruction; and

allowing execution of the finite state machine if a predefined value in a field in the microinstruction is detected and preventing execution of the finite state machine when the predefined value is not detected.

12. (New) The digital processor of claim 1, wherein the predefined value is represented by a single bit.

13. (New) The digital processor of claim 1, wherein a bit value of 0 prevents FSM execution, wherein a bit value of 1 enables FSM execution.

14. (New) The digital processor of claim 1, wherein when FSM execution is enabled a predetermined field in the microinstruction is used to invoke FSM processing.

15. (New) The digital processor of claim 14, wherein when FSM execution is prevented the predetermined field in the microinstruction is used for a purpose other than to invoke FSM processing.

16. (New) The digital processor of claim 1, wherein multiple instructions are used for FSM control.

17. (New) The digital processor of claim 16, wherein a predetermined field is used to indicate how many microinstructions are to be used for FSM control.